

Application Serial No. 10/811,768
Reply to office action of June 14, 2007

SEP 14 2007 PATENT
Docket: CU-3664

Amendments To The Claims

The listing of claims presented below will replace all prior versions, and listings, of claims in the application.

Listing of claims:

1. (withdrawn) A method of manufacturing a semiconductor device substrate, said method comprising the steps of:
arranging on a base a temporary fixing member for temporarily fixing an electronic component;
temporarily fixing the electronic component on the base by using the temporary fixing member;
forming a substrate body on the base and the electronic component;
removing at least a portion of the base which portion corresponds to the electronic component, thereby exposing the temporary fixing member; and
removing the temporary fixing member, thereby enabling the electronic component to make an external connection.
2. (withdrawn) The method as claimed in claim 1, wherein the temporary fixing member is made of a metal.
3. (withdrawn) The method as claimed in claim 2, wherein the metal is a low-melting metal.

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4. (withdrawn) The method as claimed in claim 1, wherein the temporary fixing member is a sheet member configured to be able to bond the electronic component to the base.
5. (withdrawn) The method as claimed in claim 4, wherein the sheet member is a thermo peeling tape.
6. (withdrawn) The method as claimed in claim 4, wherein the sheet member is a water-soluble sheet.
7. (withdrawn) The method as claimed in claim 4, wherein the sheet member is a UV tape.
8. (withdrawn) The method as claimed in claim 1, wherein the temporary fixing member is a liquid adhesive.
9. (withdrawn) The method as claimed in claim 1, wherein the step of removing at least the portion of the base removes the entire base.
10. (currently amended) A semiconductor device substrate, comprising:
a substrate layer including an insulating layer and an interconnection layer, said insulating layer and said interconnection layer being stacked;
an electronic component buried in the insulating layer, a bump being formed on

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said electronic component acting as an electrode of the electronic component; and

a base layer that is disposed in contact with the insulating layer of the substrate layer, and said base layer having an opening formed at a portion corresponding to the electronic component ~~to expose at least an end of the bump to accommodate an~~ externally provided semiconductor element, at least an end of the bump being exposed in the opening for connection of the electronic component to the semiconductor element in the opening.

11. (previously presented) The semiconductor device substrate as claimed in claim 10, wherein the bump projects through said substrate layer so as to be connectable to an externally provided semiconductor element.

12. (previously presented) The semiconductor device substrate as claimed in claim 10, wherein the bump projects from a surface of said electronic component facing the opening so as to be connectable to an externally provided semiconductor element.

13. (previously presented) The semiconductor device substrate as claimed in claim 10, wherein the substrate layer has a depressed portion between the opening and the electronic component to expose the bump.

14. (withdrawn) A semiconductor device, comprising:
a semiconductor device substrate including:
a substrate layer including an insulating layer and an interconnection layer, said

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insulating layer and said interconnection layer being stacked;

an electronic component buried in the insulating layer, a bump being formed on said electronic component acting as an electrode of the electronic component; and

a base layer that is in contact with the insulating layer of the substrate layer and having an opening formed at a portion corresponding to the electronic component to expose at least an end of the bump; and

a semiconductor element mounted on said semiconductor device substrate and electrically connected to the bump of said electronic component.

15. (withdrawn) The semiconductor device as claimed in claim 14, wherein the bump of said electronic component projects through said substrate layer.

16. (withdrawn) The semiconductor device as claimed in claim 14, wherein the bump of said electronic component projects from a surface of said electronic component that faces the opening.

17. (withdrawn) The semiconductor device as claimed in claim 14, wherein the substrate layer has a depressed portion between the opening and the electronic component.

18. (withdrawn) A semiconductor device substrate, comprising:
a substrate layer including an insulating layer and an interconnection layer, said insulating layer and said interconnection layer being stacked;

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an electronic component buried in the insulating layer, a bump being formed on said electronic component acting as an electrode of the electronic component; and

a base layer that is in contact with the insulating layer of the substrate layer and having an opening formed at a portion corresponding to the electronic component to expose at least an end of the bump,

wherein the substrate layer has a depressed portion between the opening and the electronic component to expose the bump.

19. (withdrawn) The semiconductor device substrate as claimed in claim 18, wherein the bump projects into the depressed portion.

20. (withdrawn) The semiconductor device substrate as claimed in claim 18, wherein a top of the bump is substantially uniform with a surface of the substrate layer that faces the opening of the base layer.

21. (withdrawn) A semiconductor device, comprising:

a semiconductor device substrate including:

a substrate layer including an insulating layer and an interconnection layer, said insulating layer and said interconnection layer being stacked;

an electronic component buried in the insulating layer, a bump being formed on said electronic component acting as an electrode of the electronic component; and

a base layer that is in contact with the insulating layer of the substrate layer and having an opening formed at a portion corresponding to the electronic component to

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expose at least an end of the bump,

wherein the substrate layer has a depressed portion between the opening and the electronic component to expose the bump; and

a semiconductor element mounted on said semiconductor device substrate and electrically connected to the bump of said electronic component.

22. (withdrawn) The semiconductor device as claimed in claim 21, wherein the bump projects into the depressed portion.

23. (withdrawn) The semiconductor device as claimed in claim 21, wherein a conductive member is provided between the bump and an electrode of the semiconductor element.